C2

pattern being isolated from a second higher interconnect pattern which intersects said interconnect pattern.

Please add new claim 41 as follows:

41. (New) A semiconductor integrated circuit including a plurality of basic cells arranged in the same direction,

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wherein each basic cell is composed of an N-channel transistor and a P-channel transistor, and

a gate of at least one of said N-channel transistor and said P-channel transistor of each cell is in a hooked shape having a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in the other sideward direction at a lower portion thereof.

REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended claim 22, 23 and 26-27 so as to clarify the subject matter of the present invention. In addition, new claim 41 has been added. No new matter has been added. It is noted that with the exception of new claim 41, the instant Preliminary Amendment is the same as the

amendment filed on January 15, 2003, which was not entered by the Examiner.

For the reasons set forth below, it is respectfully submitted that all of the pending claims satisfy the requirements of 35 U.S.C. § 112, second paragraph, and that the claims are patentable over the cited prior art references.

Applicants acknowledge and appreciate the Examiner's indication of allowable subject matter being recited by claims 34-37.

Also submitted herewith are corrected formal drawings, which revised Figs. 30-41 to include the legend "Prior Art".

Finally, it is noted that Applicants' previous amendment also included claims 38-40, which do not appear to be address in the pending Office Action. However, as each of these claims is dependent on claims 34-37, it is respectfully submitted that claims 38-40 are also in condition for allowance. In the next paper issued in this application, the Examiner is respectfully requested to indicate the status of claims 38-40.

II. The Rejection Of Claims 22-33 Under 35 U.S.C. § 112, First Paragraph

Claims 22-33 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification is such a way so as to reasonably convey to one of skill in the art that the Applicants had possession of the invention. Applicants respectfully submit that the amendments to claims 22 and 27,

which are explained below, overcome the pending rejection, and make clear the intended subject matter of the invention.

As recited by claim 22, the present invention relates to the structure of a basic CMOS cell contained in a gate array integrated circuit having a plurality of such cells. As is known, the basic cells are interconnected with one another in various manners to formed the desired circuits. Figs. 1A and 1C illustrate the structure of the basic CMOS cell as recited by claim 22. As shown, the exemplary cell comprises n-channel transistors (TN1 and TN2) and p-channel transistors (TP1 and TP2) and interconnects 53 and 54 connected to the gate electrode (2A and 2B) of the p-channel transistor TP1 and the n-channel transistor TN1, respectively. In addition, each cell comprises an interconnect pattern, which is identified by reference numeral 9 in Fig. 1A, which is formed in the uppermost interconnect layer of the basic cell (i.e., as shown in Fig. 1F it is possible for the basis cell to comprises multiple layers of interconnections (e.g., 54, 56), the interconnect pattern 9 is formed in the uppermost layer).

Importantly, the interconnect pattern 9 is not coupled to the n-channel transistor, the p-channel transistor or the interconnect coupled to the transistors. Thus, the interconnect pattern is isolated from the contact hole (55 and 56) and interconnect (53 and 54) contained in the basic cell that are coupled to the transistors. However, while isolated from these elements, the interconnect pattern 9 is utilized to couple global

interconnects, which are disposed above the basic cell, to one another.

For example, as shown in the annotated version of Fig. 3A enclosed herewith, the gate 3A1 of cell 1A is coupled to the gate 3A2 of cell 1D utilizing global interconnect X. However, in making this connection, the interconnection pattern 9 of cell 1D is utilized to form part of the global interconnect X (*see, also*, page 11, lines 11-21 of the specification).

Thus, in the basic cell, the interconnect pattern 9 is electrically isolated from the interconnect and contact hole contained in the same cell. The interconnect pattern 9 is utilized to connect global interconnects extending over the basic cell to one another. In this regard, it is noted that it is possible for the interconnect pattern 9 to be coupled to a transistor via a global interconnect. However, the interconnect pattern 9 is isolated from the interconnect and contact hole within the given basic cell.

For all of the foregoing reasons, it is respectfully submitted that interconnect pattern 9 is properly referred to as an "interconnect", and should not be simply a metal layer.

With regard to the rejection of claim 25, the claim is intended to cover the subject matter disclosed for example in Fig. 11A. As shown therein, the interconnect pattern 9 of adjacent cells (e.g., 1A and 1B) can be connected together. It is noted that the interconnect patterns remain isolated from the contact hole and the interconnect of

each given cell. As such, it is submitted that claim 25 is fully supported by the specification and would be readily understandable by one of skill in the art.

With regard to claim 27, this claim has been amended to recite that the interconnect pattern is coupled to a first higher interconnect pattern that intersects the interconnect pattern and is electrically isolated from a second higher interconnect pattern that intersects the interconnect pattern. For example, referring to enclosed Fig. 3A, the interconnect pattern 9 of cell 1C is coupled to interconnect A, which is formed in a higher level, but it is not coupled to interconnect B, which intersects interconnect pattern 9 and which is formed in the same level as interconnect A. It is submitted that, as amended, claim 27 satisfies all requirements of 35 U.S.C. § 112.

For all of the foregoing reasons, it is respectfully submitted that all pending claims comply with the requirements of 35 U.S.C. § 112, first paragraph.

III. The Rejection Of The Claims In View Of Amishiro

Claims 22 and 23 were rejected under 35 U.S.C. § 102 in view of USP No. 6,288,477 to Amishiro. Applicants respectfully submit that claims 22 and 23 are not anticipated by Amishiro for at least the following reasons.

The structure of the claimed CMOS basic cell as recited by claim 22 is detailed above. Importantly, as noted above, the interconnect pattern 9 is isolated from the

contact holes and the interconnects contained in the same basic cell.

Turning to the cited prior art, it is asserted that the interconnect 10D of Amishiro corresponds to the claimed interconnect pattern 9. It is respectfully submitted that this conclusion is in error. As shown in Figs. 5 and 6, interconnect 10D of Amishiro is not isolated from the contact holes or the interconnects coupled to the transistor. Indeed, interconnect 10D of Amishiro corresponds to interconnect 54 as shown for example in Fig. 1G of the present invention. Thus, at a minimum, Amishiro fails to disclose the foregoing limitation recited by claim 22 that the interconnect pattern 9 be isolated from the contact holes and the interconnects contained in the basic cell.

Accordingly, as anticipation under 35 U.S.C. § 102 requires that each element of the claim in issue be found, either expressly described or under principles of inherency, in a single prior art reference, ***Kalman v. Kimberly-Clark Corp.***, 713 F.2d 760, 218 USPQ 781 (Fed. Cir. 1983), for at least the foregoing reasons, it is clear that Amishiro does not anticipate any of new claims 22 and 23.

IV. The Rejection Of The Claims 24-33 Under 35 U.S.C. § 103

Claims 24-33 were rejected under 35 U.S.C. § 103 in view of Amishiro in view of Applicants' Admitted Prior Art.

As each of claims 24-33 incorporate the limitations of claim 22 therein, for at

least the same reasons as set forth above, it is respectfully submitted that, at a minimum, Amishiro fails to disclose or suggest a basic cell having an interconnect pattern isolated from the contact holes and the interconnects contained in the basic cell. Further, the AAPA is neither relied upon as disclosing this aspect of the present, nor does it. Accordingly, for at least the same reasons as set forth above, the combination of Amishiro and the AAPA fails to disclose or suggest each and every limitation of the claimed invention.

Thus, as each and every limitation must be disclosed or suggested by the combination of prior art (see, M.P.E.P. § 2143.03) in order to establish a *prima facie* case of obviousness, and the combination of Amishiro and the AAPA fails to do so, it is respectfully submitted that claims 24-33 are patentable over the cited prior art.

V. Request For Notice Of Allowance

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

Date: 3/14/03 By: _____

Michael E. Fogarty
Registration No. 36,139

600 13th Street, N.W., Suite 1200
Washington, DC 20005-3096
Telephone: (202) 756-8000
Facsimile: (202) 756-8087

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims 22, 23, 26 and 27 have been amended and new claim 41 has been added as follows:

22. (Amended) A CMOS basic cell comprising:

an N-channel transistor, [and] a P-channel transistor and an interconnect connected to said N-channel or P-channel transistor through a contact hole on a semiconductor substrate; and

an interconnect pattern which is electrically isolated from said contact hole and said interconnect and which exists between said N-channel transistor and said P-channel transistor,

wherein said interconnect pattern is formed in an uppermost interconnect layer of said CMOS basic cell.

23. (Amended) The [CMQS] CMOS basic cell of Claim [1] 22, wherein said interconnect pattern extending either along a perpendicular direction or along a horizontal direction relative to a boundary between said N-channel transistor and said P-channel transistor.

26. (Amended) [The gate array semiconductor integrated circuit] The CMOS basic cell of any one of Claims 22 to 25, wherein two or more said CMOS basic cells are electrically connected by a higher interconnect pattern located in a layer that is higher than said interconnect pattern.

27. (Amended) [The gate array semiconductor integrated circuit] The CMOS basic cell according to Claim 26, wherein said higher interconnect pattern is located in a region between said P-channel transistors and said N-channel transistors except the both ends of said interconnect pattern, and

wherein said interconnect pattern which intersects said higher interconnect pattern is electrically connected with [a] said higher interconnect pattern, said interconnect pattern being isolated from a second [except said] higher interconnect pattern which intersects said interconnect pattern.

--41. (New) A semiconductor integrated circuit including a plurality of basic cells arranged in the same direction,

wherein each basic cell is composed of an N-channel transistor and a P-channel transistor, and

a gate of at least one of said N-channel transistor and said P-channel

transistor of each cell is in a hooked shape having a first bent part bending in one sideward direction at an upper portion thereof and a second bent part bending in the other sideward direction at a lower portion thereof.--